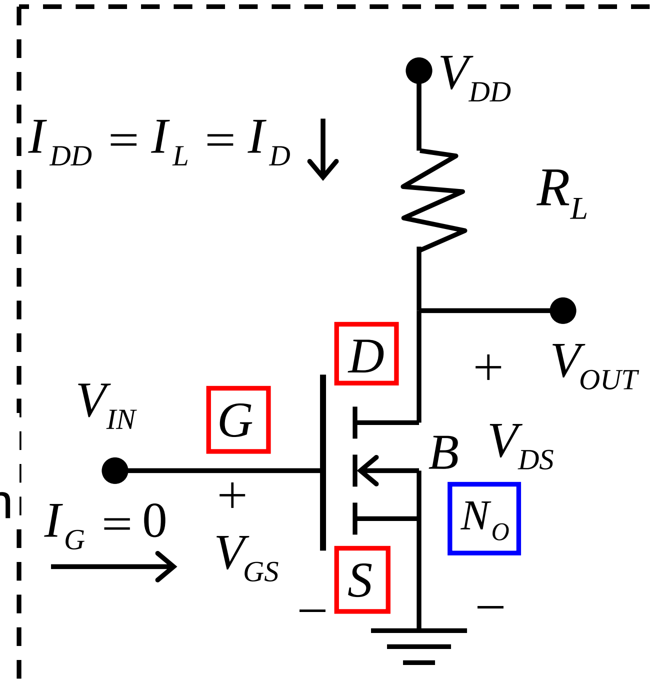
Digital Electronics.

CHAPTER EIGHTTEEN

MOS Digital Integrated Circuits

Power Dissipation of Resistor Loaded NMOS Inverter

The currents supplied by V_{DD} for <u>high</u> and <u>low</u> states must be determined



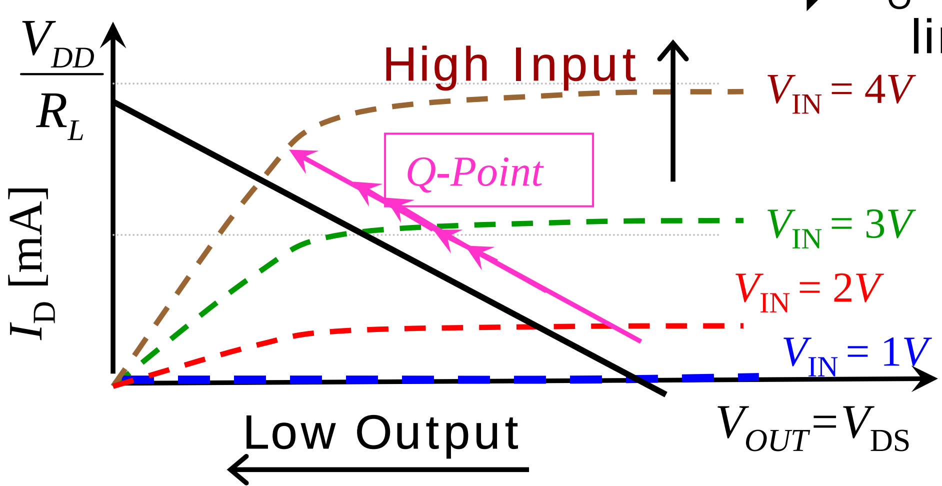
Output high current supplied $I_{DD}(OH)$

For High output, Input is <u>low</u> ➡ N_O is OFF

$$\boxed{I_{DD}(OH) = 0}$$

Output low current supplied $I_{DD}(OL)$

For Low output, Input is <u>high</u> ➡ N_O operates in linear region



Power Dissipation of Resistor Loaded NMOS Inverter

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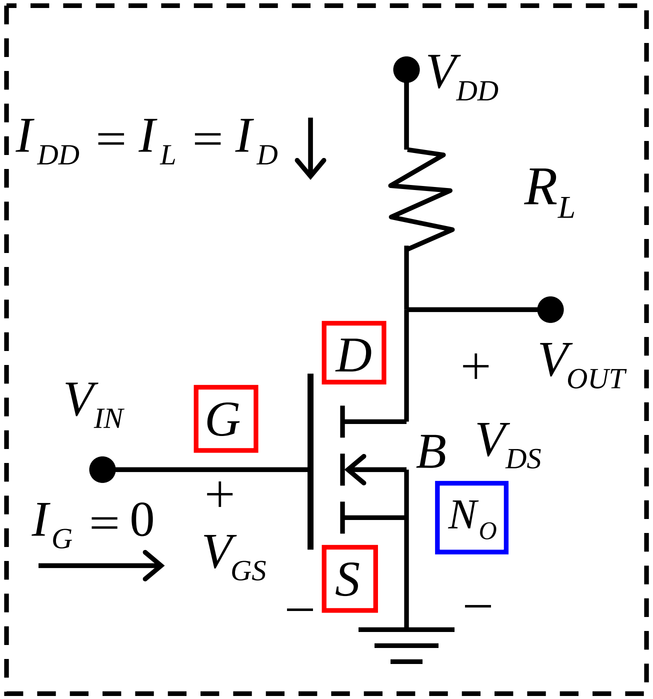
$I_{DD}(OL)$ ⇒ N_O operates in linear region $\boxed{V_{GS} = V_{OH} = V_{DD}}$ $\boxed{V_{DS} = V_{OL}}$

$$I_D = \frac{K_n}{2}\left[2\times(V_{DD}-V_{TN})V_{DS} - V_{DS}^2\right] = \frac{V_{DD}-V_{DS}}{R_L}$$

$$\boxed{V_{DS} = V_{OL} \cong \frac{V_{DD}}{(V_{DD}-V_{TN})K_nR_L+1} = \underbrace{V_{DS} \le (V_{GS}-V_{TN})}_{\text{To ensure that } N_O \text{ operates in linear mode}}}$$

Slide 8 of last chapter



$$I_{DD}(OL) = \frac{K_n}{2}\left[2\times(V_{DD}-V_{TN})V_{OL} - V_{OL}^2\right]$$

Static Power Dissipation $P_{DD}(avg)$

$$P_{DD}(avg) = V_{DD}\left(\frac{I_{DD}(OL)+I_{DD}(OH)}{2}\right) = V_{DD}\left(\frac{I_{DD}(OL)}{2}\right)$$

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Dynamic Power Dissipation $P_{DD}(dyn)$

$$\boxed{P_{DD}(dyn) = C_L \upsilon (V_{DD})^2}$$

C_L is the total load capacitance at the output of the gate

υ is the switching frequency of the gate

Power Dissipation of Resistor Loaded NMOS Inverter

- Example

(a) Calculate the static dissipated power in the driver gate for the last example

$V_{DD}=5V$, $V_T=1$ V, $k_n=40\mu A/V^2$, $R_L=50k\Omega$,

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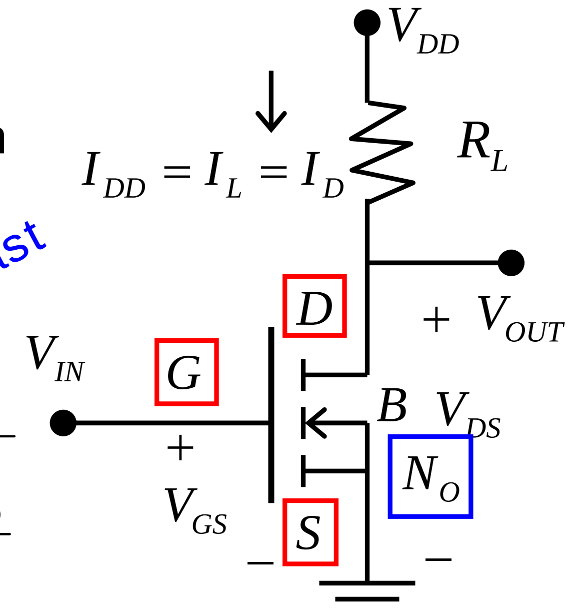


- Solution (Exact Sol.)

$$V_{OL}=\left[V_{DD}-V_{TN}+\frac{1}{K_nR_L}\right]\pm\sqrt{\left[V_{DD}-V_{TN}+\frac{1}{K_nR_L}\right]^2-\frac{2}{K_n}\frac{V_{DD}}{R_L}}$$

$$V_{OL}=4.5\pm3.905 \qquad V_{OL}=0.595V \qquad V_{OL}=\cancel{8.41}V$$

$$\underbrace{\boxed{V_{OL}=V_{DS}\le\left(V_{GS}-V_{TN}\right)}}_{} \quad \boxed{V_{OL}=V_{DS}\le(5-1)}$$

To ensure that N_O operates in linear mode

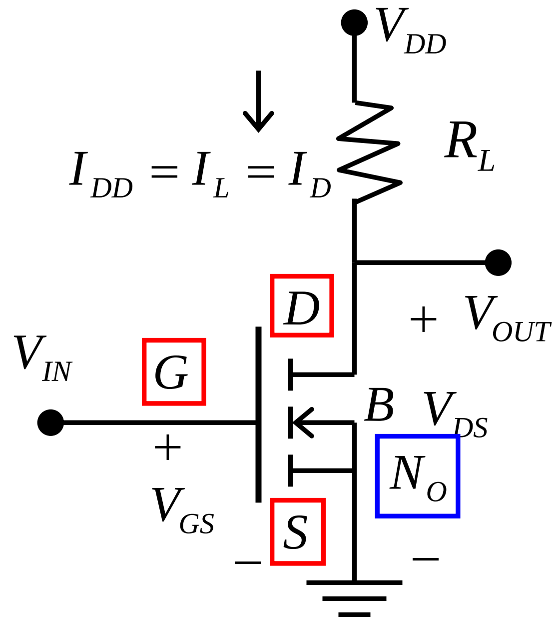
Power Dissipation of Resistor Loaded NMOS Inverter

Cont.

- Example

(a) Calculate the static dissipated power in the driver gate for the last example

$V_{DD}=5V$, $V_T=1$ V, $k_n=40\mu A/V^2$, $R_L=50k\Omega$,



- Solution (Exact Sol.)

$$V_{OL}=0.595V$$

$$I_{DD}(OL)=\frac{V_{DD}-V_{OL}}{R_L}=\frac{5-0.595}{50k}=88.1\mu A$$

$$I_{DD}(OL)=\frac{K_n}{2}\left[2\times(V_{DD}-V_{TN})V_{DS}-V_{DS}^2\right]=20\times10^{-6}\left(2\times4\times0.595-0.595^2\right)=88.1\mu A$$

$$\boxed{P_{DD}(avg)=5\left(\frac{88.1}{2}\right)=0.22mW}$$

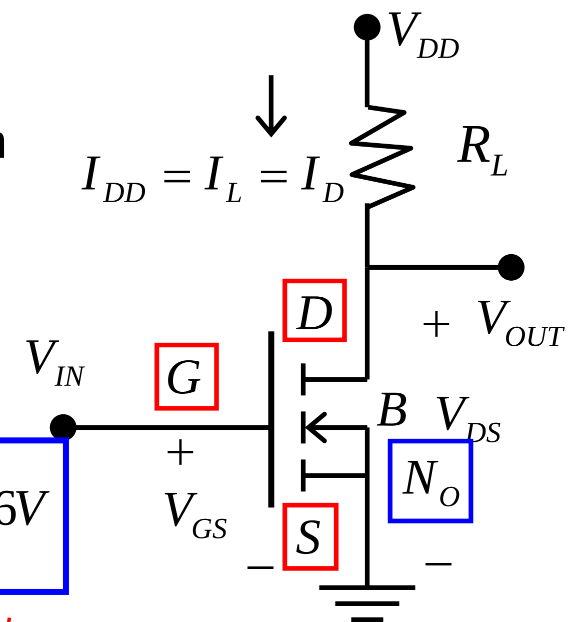
Power Dissipation of Resistor Loaded NMOS Inverter

Cont.

- Example

(a) Calculate the static dissipated power in the driver gate for the last example

$V_{DD}=5V$, $V_T=1$ V, $k_n=40\mu A/V^2$, $R_L=50k\Omega$,



- Solution (Approx. Sol.)

$$\boxed{V_{OL}\cong\frac{V_{DD}}{(V_{DD}-V_{TN})K_nR_L+1}=\frac{5}{(5-1)\times40\times10^{-6}\times50\times10^{3}}=0.556V}$$

$$I_{DD}(OL)=\frac{V_{DD}-V_{OL}}{R_L}=\frac{5-0.556}{50k}=88.89\mu A$$

Diff. due to approx.

$$I_{DD}(OL)=\frac{K_n}{2}\left[2\times(V_{DD}-V_{TN})V_{DS}-V_{DS}^2\right]=20\times10^{-6}\left(2\times4\times0.556-0.556^2\right)=82.8\mu A$$

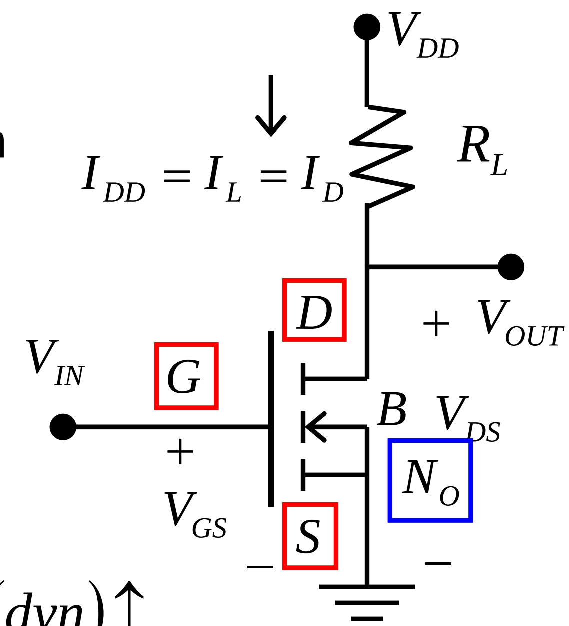
$$\boxed{P_{DD}(avg)=5\left(\frac{82.8}{2}\right)=0.207mW}$$

Power Dissipation of Resistor Loaded NMOS Inverter

Cont.

- Example

(b) Calculate the dynamic dissipated power in the driver gate for the last example
$V_{DD}=5V$, $V_T=1$ V, $k_n=40\mu A/V^2$, $R_L=50k\Omega$,
$C_L=1$ pF, and $\upsilon = 1MHz$



- Solution

$$P_{DD}(dyn) = C_L \upsilon (V_{DD})^2$$

$$C_L \uparrow \Rightarrow P_{DD}(dyn) \uparrow$$

$$P_{DD}(dyn) = 10^{-12} \times 10^6 \times 25 = 25\mu W$$

$$C_L = C'_{G1} + C'_{G2} + \cdots$$ *parallel*

Note: In resistor loaded NMOS inverter, the dynamic dissipated power is less than the static dissipated power

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- HW #10:Solve Problems: 18.**1-3**,